Sub-5-nm Monolayer Silicane Transistor: A First-Principles Quantum Transport Simulation

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As one of the thinnest forms of semiconducting silicon, monolayer (ML) silicane has not only excellent gate electrostatics and carrier transport ability, but also compatibility with well-established silicon-based technology. We explore the device performance limits of sub-5-nm ML silicane metal-oxide-semiconductor field-effect transistors (MOSFETs) by applying *ab initio* quantum transport simulations. The on-state current, effective delay time, and power-delay product of the optimized *n*-type and *p*-type ML silicane MOSFETs can well or nearly meet the high-performance device requirements of the International Technology Roadmap for Semiconductors (ITRS) at a gate length of 5 nm. Those of the optimized *n*-type ML silicane MOSFETs at a gate length of 3 nm and the *p*-type ML silicane MOSFETs at a gate length of 5 nm can meet the low-power-device demands of the ITRS. Thus, ML silicane as channel materials can scale the Moore's law down to 5 nm.

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I. INTRODUCTION

The scaling of transistors has improved their performance and increased the functionality of the circuit from one generation to the next in the past half-century [1]. The trend is ending as the gate length approaches sub-10-nm regimes for traditional bulk silicon, because such a short channel suffers from unavoidable high heat dissipation and short-channel effects [2]. To extend the gate length down to the sub-10-nm regime, semiconductor materials beyond traditional bulk silicon are extensively explored. Among the various alternative channel materials for transistors, two-dimensional (2D) semiconductors show great potential because of their excellent gate electrostatics in atomically thin crystals and improved carrier transport in the dangling-bond-free smooth surface [3–5]. 2D MoS_2, as the most famous member of the transition-metal dichalcogenides (TMDs), is first prepared as field-effect transistors (FETs) with channel lengths down to the sub-10-nm regime [6–8]. The on:off ratio of 2D MoS_2 FETs can be up to 10^6, but the on-state current is less than 250 μA/μm, which does not reach the International Technology Roadmap for Semiconductors (ITRS) standard for a high-performance (HP) device. It is theoretically predicted that the on-state current of black phosphorene and 2D InSe can satisfy the HP and low-power (LP) requirements of the ITRS in the sub-10-nm region [9,10], and the carrier mobility is up to 1000 $cm^2\ V^{-1}\ s^{-1}$ in experimentally fabricated FETs [11–14]. However, there are no experimental reports of sub-10-nm FETs for these materials, and the instability of black phosphorene and InSe in air is an issue that remains to be solved. Therefore, there is an urgent need to explore other 2D materials with excellent performance, air stability, and compatibility with existing technology.

Compared with other 2D semiconductors, 2D silicon material has superior compatibility with well-established silicon-based technology. Monolayer (ML) forms of silicon, which includes silicene and silicane, can be considered as the limit of ultrathin silicon with one layer of silicon atoms [15]. ML silicene, analogous to graphene, comprises sp^2- and sp^3-hybridized Si atoms and a

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low-buckled structure with excellent electronic properties [16]. However, its zero-gap semimetallic character and extreme instability hinder silicene's application in transistors. Although applying an electric field and adsorption-intercalation of metal atoms are used to open up its band gap, it is still less than 0.4 eV, which cannot fulfill the requirements of a logic device [17,18]. ML silicane comprises sp^3-hybridized Si atoms, and thus, has higher stability than that of silicene [19,20]. Layered silicane is successfully synthesized by the reaction of $CaSi_2$ with HCl [21], and ML hydrogenated half-silicane (one Si sublattice fully H saturated and the other sublattice intact) is also produced on Ag(111) substrates [22,23]. The chairlike configuration is predicted to be the most stable configuration of hydrogenated ML silicane, in which H atoms are alternating on both sides of the plane [24–26]. Unlike silicene, chairlike hydrogenated ML silicane (hereafter called ML silicane) possesses semiconducting characteristics, with an indirect band gap of about 2.20 eV and a small electron and hole effective mass of about 0.1 m_e. Thus, ML silicane is a promising channel candidate with excellent compatibility with the present silicon-based technology.

Theoretical attempts using the semiclassical (SC) method are made to study the transport performances of sub-10-nm ML silicane metal-oxide-semiconductor FETs (MOSFETs) [27,28]. It is found that both *n*- and *p*-type MOSFETs of ML silicane offer a better on-state current than those of transistors made of 2D TMDs. Unfortunately, the parameter-dependent SC method will induce a large error in ultrashort devices. The error first originates from the parameter-dependent transition matrix element. Second, the SC method chiefly centers on the channel electrostatics and neglects the interaction between the electrode regime and the channel regime [17,29]. Third, the previously used SC ballistic transport model does not capture the subthreshold leakage current from band-to-band tunneling (BTBT) [27]. Hence, a parameter-free *ab initio* quantum transport simulation is highly desirable to describe the transport performance limit of the sub-5-nm ML silicane MOSFET.

Here, we explore the performance limit of double-gated (DG) sub-5-nm ML silicane MOSFETs on the basis of precise *ab initio* quantum transport simulation. The on-state current of the optimized *n*-type ML silicane HP MOSFET (5 nm) is 1374 μA/μm, which is 5 times larger than that of its ML MoS_2 counterpart (230 μA/μm) [30] and comparable to that of its ML InSe counterpart [10]. The optimized *n*-type and *p*-type ML silicane MOSFETs can reach, or nearly reach, the ITRS demands for both HP and LP devices for the on-state current, effective delay time, and power-delay product until the gate length is scaled down to 5 nm or even 3 nm (for the *n*-type LP device). Therefore, ML silicane is a promising channel material for the sub-5-nm transistor, owing to its compatibility with existing silicon semiconductor technology and high device performances.

II. METHODS

The geometric optimization and electronic structures are calculated by density-functional theory (DFT) with the projector augmented wave (PAW) method [31], which is implemented in the VASP package [32,33]. A plane-wave basis set with a cutoff energy of 500 eV is used. Atomic positions are fully optimized until the forces are smaller than 10^{-2} eV/Å, and the energy is converged to less than 10^{-5} eV between two iteration steps. The transport properties are calculated by applying DFT, combined with the nonequilibrium Green's function (NEGF) formalism, as implemented in the Atomistix ToolKit (ATK) 2019 package [34,35]. According to the Landauer-Bűttiker formula, the drain current, I_{DS}, at a given bias voltage, V_b, and gate voltage, V_g, is calculated as follows:

$$I_{DS}(V_b, V_g) = \frac{2e}{h}\int_{-\infty}^{+\infty}\{T(E, V_b, V_g)[f_S(E-\mu_S) - f_D(E-\mu_D)]\}dE, \quad (1)$$

where $T(E, V_b, V_g)$ is the transmission coefficient; f_S and f_D are the Fermi-Dirac distribution functions for the source and drain, respectively. μ_S and μ_D are the electrochemical potentials for the source and drain, respectively.

The transmission coefficient $T(E)$ is the average of *k*-dependent transmission coefficients over the Brillouin zone. The *k*-dependent transmission coefficients $T_{k\|}(E)$ at given energy E is represented by

$$T_{k_\|}(E) = Tr[\Gamma^l_{k\|}(E)G_{k\|}(E)\,\Gamma^r_{k\|}(E)G^\dagger_{k\|}(E)], \quad (2)$$

where $G^\dagger_{k\|}(E)$ and $G_k(E)$ are the advanced and retarded Green's function, respectively, and $\Gamma^{l/r}_{k\|}(E) = i(\sum_{l/r} - \sum^\dagger_{l/r})$ defines the level broadening from the left and right electrodes in the form of self-energy $\sum_{l/r}$. The double-ξ polarized (DZP) basis set is used. The real-space mesh cutoff is taken as 75 hartrees, and the temperature is set to 300 K. The *k*-point grids in the form of Monkhorst-Pack are set to $50 \times 1 \times 1$ and $50 \times 1 \times 50$ for the central region and the electrode region, respectively [36]. The boundary condition along the transverse, vertical, and transport directions is of periodic, Neumann, and Dirichlet type, respectively [37].

The generalized gradient approximation (GGA) in the form of the Perdew-Burke-Ernzerhof (PBE) potential is used to describe the exchange-correlation interaction in all calculations [38]. Because the electron-electron interaction of the channel region is greatly screened by doping carriers from the electrode region, the DFT GGA method based on single-electron approximation is exhaustive enough to pick

up the electron behavior in a FET configuration. This is proved by the consistency of the subthreshold swing (SS) between the observation (65 mV/dec) and the simulation (66 mV/dec) in the subthreshold region for the 1-nm-gate 2D MoS_2 device [39,40]. Additionally, it is also proved by the agreement of the band gap of the degenerately doped ML $MoSe_2$, which is 1.52 eV at the DFT GGA level [41], 1.59 eV at the high-level *GW* method [42], and 1.58 eV obtained by angle-resolved photoemission spectroscopy [43].

III. RESULTS AND DISCUSSIONS

A. Structure and device optimization

The atomic structure of ML silicane is shown in Fig. 1(a). The optimized lattice constant of ML silicane is 3.89 Å, which is consistent with previous theoretical results [24]. The energy band structure and density of states (DOS) of ML silicane are plotted in Fig. 1(b), and an indirect band gap of 2.18 eV is obtained with the valance-band maximum (VBM) and conduction-band minimum (CBM) located at the Γ and *M* points, respectively, which coincide with previous reports [24,26]. The electron states at the CBM are mainly from the *s* orbital, while that at the VBM is mainly from the $p_x + p_y$ orbitals. The effective masses, m^*, at the VBM and the CBM along the high symmetry lines are extracted from the band structures, according to the equation $1/m^* = (1/\hbar^2)(d^2E/dk^2)$. The band along the $M \rightarrow K$ direction is sharper than that along the $M \rightarrow \Gamma$ direction at the CBM; therefore, the electron effective mass along the $M \rightarrow K$ direction (0.118 m_e, m_e is the mass of an electron) is smaller than that along the $M \rightarrow \Gamma$ direction (3.209 m_e). The energy variation at the VBM along the $\Gamma \rightarrow M$ and $\Gamma \rightarrow K$ directions are similar; thus, the hole effective masses, along with Γ, point to other directions that are rather isotropic. The valance bands are degenerate at the VBM, which lead to heavy and light hole effective masses, with values of about 0.577 and 0.123 m_e, respectively. The small electron and hole effective masses of ML silicane ensure its high carrier mobility [44]. We also calculate the band structure of ML silicane by using the DZP basis set in the ATK package, which is the same as that obtained by using the plane-wave basis set in VASP (see the Supplemental Material for the band structure obtained by using the DZP basis set [45]).

Two-probe DG ML silicane MOSFETs are constructed with intrinsic ML silicane as the channel and *n*- or *p*-doped ML silicane as the electrodes of semi-infinite length, as illustrated in Fig. 2(a). Underlap (UL) between the electrode and the gate can improve the device performance, and thus, it is used in the device models. The channel length, L_{ch}, is the sum of the gate length, L_g, and twice the length of the underlap, i.e., $L_{ch} = L_g + 2\text{UL}$. We use the atomic compensation charges method (see the Supplemental Material for details [45]) for doping in the electrodes, in which extra charge is introduced by modifying the densities of the individual atoms. The doping concentration of the carriers and the length of the UL are tested for the LP device with a gate length of 5 nm, as shown in Figs. 2(b) and 2(c). The doping concentration is tested with values of 1.0×10^{12}, 5.0×10^{12}, 1.0×10^{13}, and 5.0×10^{13} cm^{-2}. Although the current at a doping concentration of 5.0×10^{13} cm^{-2} is higher than those at other doping concentrations, it is hard to get a current lower than 0.1 μA/μm at this high doping concentration. Hence, a doping concentration of 1.0×10^{13} cm^{-2} is used here, unless otherwise specified. The lengths of the symmetric UL are chosen to be 0, 2, and 4 nm.

B. On-state current

The on-state current, I_{on}, and off-state current, I_{off}, are crucial figures of merit to evaluate the performance of logic devices. In the recent version of ITRS and the 2018 version of international roadmap for devices and systems (IRDS), the technical node range reaches 1.5 nm; however, the physical gate length is not less than 10 nm. There are no data for comparison at the sub-5-nm gate-length region,

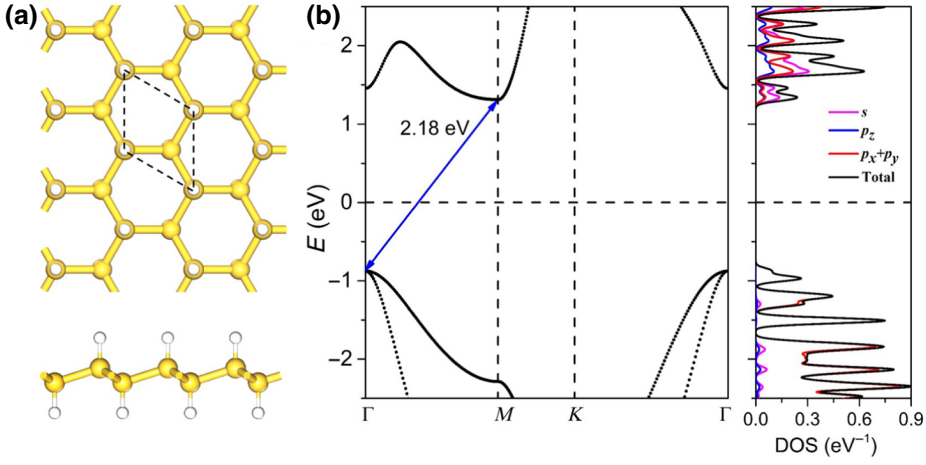

FIG. 1. Crystal and electronic structures of ML silicane. (a) Top and side views of ML silicane. Dashed lines represent the primitive unit cell of ML silicane. Yellow and white balls represent silicon and hydrogen atoms, respectively. (b) Band structures and density of states of ML silicane.

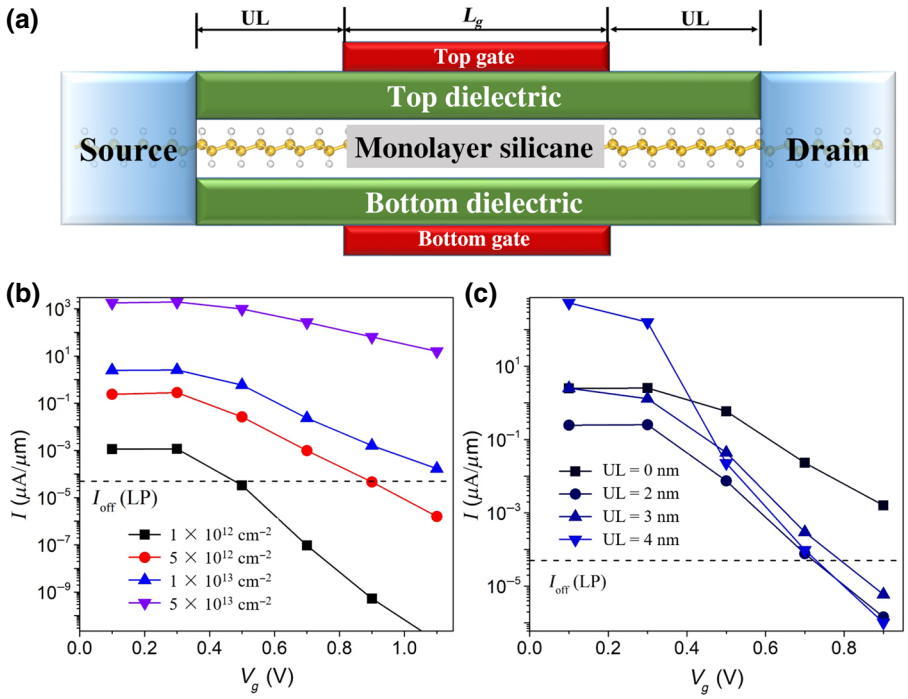

FIG. 2. (a) Schematic view of the DG ML silicane MOSFET. Transfer characteristics for (b) different electrode doping concentrations (UL = 0 nm) and (c) different UL lengths (doping concentration of 1.0×10^{13} cm^{-2}) at a gate length of 5 nm.

so we compare our results with the requirements of ITRS 2013. Following the requirements of ITRS 2013 for the off-state current, the I_{off} of HP and LP devices is set to 0.1 and 5×10^{-5} μA/μm, respectively. The on-state current, I_{on}, is examined at a specific supply gate voltage of V_g(on-state) = $V_{DD} + V_g$(off-state), where V_{DD} is the supply voltage. According to the ITRS requirements for HP and LP devices of different gate lengths, the power-supply voltage, V_{DD}, is set to 0.64–0.66 V and the equivalent oxide thickness (EOT) of the SiO_2 dielectric is set to 0.41–0.43 nm.

The I-V characteristics of the n- and p-type sub-5-nm DG ML silicane MOSFETs are shown in Figs. 3 and 4, respectively. To read the on-state current conveniently, the I-V curves at UL = 2 and 4 nm are shifted to the same I_{off} point as that at UL = 0 nm (see Figs. S2 and S3 within the Supplemental Material [45]). The key parameters of the ballistic performance are given against the ITRS

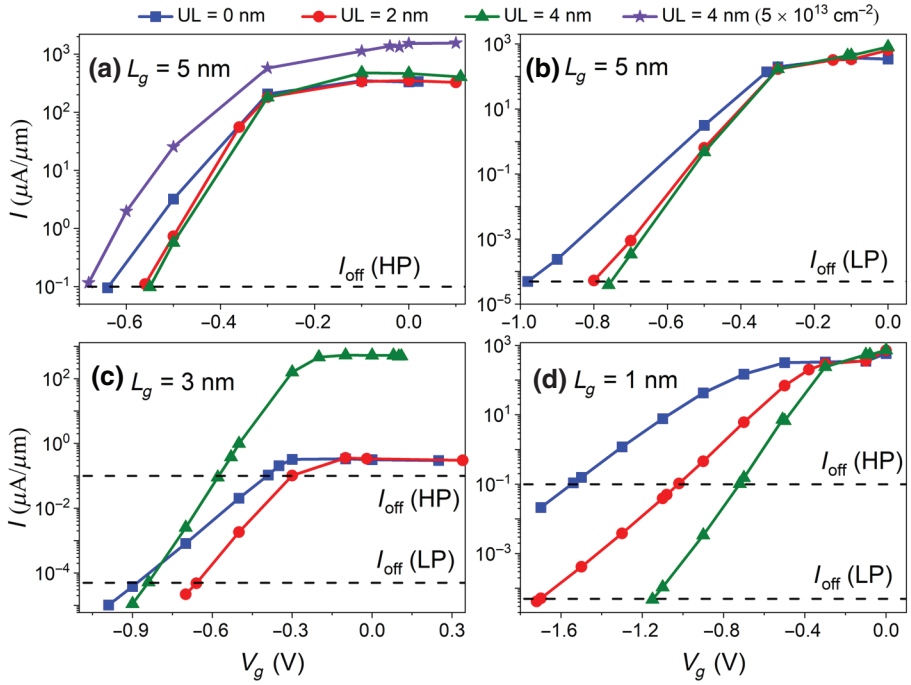

FIG. 3. Transfer characteristics for the n-type DG ML silicane MOSFETs at biases of (a) $V_b = 0.66$ V and $L_g = 5$ nm, (b) $V_b = 0.66$ V and $L_g = 5$ nm, (c) $V_b = 0.64$ V and $L_g = 3$ nm, and (d) $V_b = 0.64$ V and $L_g = 1$ nm with different lengths of UL.

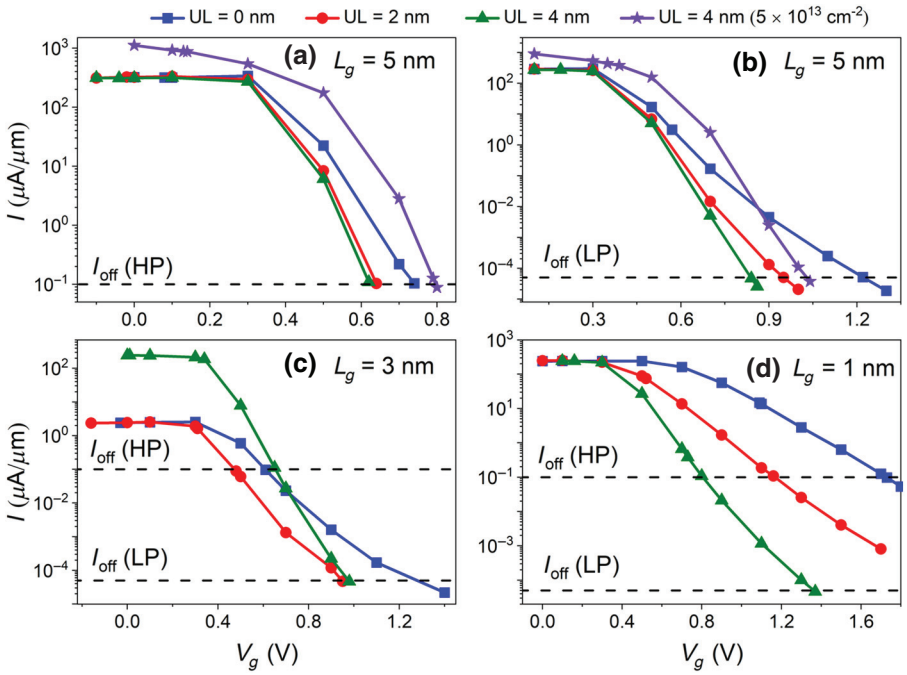

FIG. 4. Transfer characteristics for the p-type DG ML silicane MOSFETs at biases of (a) $V_b = 0.66$ V and $L_g = 5$ nm, (b) $V_b = 0.66$ V and $L_g = 5$ nm, (c) $V_b = 0.64$ V and $L_g = 3$ nm, and (d) $V_b = 0.64$ V and $L_g = 1$ nm with different lengths of UL.

requirements for the n- and p-type devices in Tables I and II. It is found that the trend of the I-V characteristics for the corresponding n- and p-type ML silicane MOSFETs are similar. The curves at the subthreshold region are greatly affected by using the length of UL. The slope of the I-V curves at the subthreshold region considerably increases with an increase of UL at gate lengths of $L_g = 3$ and 1 nm, while it slightly increases with an increase of UL at a gate length of $L_g = 5$ nm. Owing to the short-channel effect, and thus, large source-drain leakage current, the off-state current fails to meet the requirements of the ITRS for a LP device without an UL at a gate length of $L_g = 1$ nm.

TABLE I. Benchmark of the ballistic performance upper limit of the sub-5-nm DG n-type and p-type monolayer silicane MOSFETS against the ITRS 2013 requirements for HP devices in 2028. The general doping density is 1×10^{13} cm^{-2}, unless otherwise specified.

	L_g (nm)	UL (nm)	SS (mV/dec)	I_{on} (μA/μm)	I_{off} (μA/μm)	C_t (fF/μm)	τ (ps)	PDP (fJ/μm)
n-type	5	4 (5×10^{13} cm^{-2})	65	1374	0.07	0.086	0.042	0.037
		4	65	407	0.1	0.057	0.093	0.025
		2	73	326	0.11	0.127	0.258	0.055
		0	92	340	0.1	0.210	0.407	0.092
	3	4	77	527	0.09	0.039	0.047	0.016
		2	101	0.3	0.10	0.067	143.19	0.028
		0	150	0.3	0.11	0.079	169.08	0.032
	1	4	129	541	0.1	0.020	0.024	0.024
		2	178	201	0.1	0.025	0.079	0.079
		0	247	43	0.11	0.035	0.527	0.527
p-type	5	4(5×10^{13} cm^{-2})	67	871	0.09	0.099	0.075	0.043
		4	69	309	0.11	0.068	0.144	0.029
		2	73	323	0.1	0.105	0.214	0.046
		0	100	317	0.1	0.185	0.386	0.081
	3	4	81	244	0.11	0.042	0.110	0.017
		2	135	2.36	0.09	0.052	14.02	0.021
		0	140	2.41	0.1	0.071	18.95	0.029
	1	4	126	243	0.11	0.019	0.051	0.051
		2	243	74	0.11	0.029	0.250	0.250
		0	431	15	0.1	0.034	1.464	1.464
ITRS HP	5.1			900	0.1	0.60	0.423	0.24

TABLE II. Benchmark of the ballistic performance upper limit of the sub-5-nm DG *n*-type and *p*-type monolayer silicane MOSFETS against the ITRS 2013 requirements for LP devices in 2028. The general doping density is 1×10^{13} cm^{-2}, unless otherwise specified.

	L_g (nm)	UL (nm)	SS (mV/dec)	I_{on} (μA/μm)	I_{off} (μA/μm)	C_t (fF/μm)	τ (ps)	PDP (fJ/μm)
n-type	5	4	67	438	3.93×10^{-5}	0.049	0.073	0.021
		2	75	322	5.34×10^{-5}	0.084	0.169	0.035
		0	96	139	4.98×10^{-5}	0.133	0.620	0.056
	3	4	77	467	5.22×10^{-5}	0.039	0.054	0.016
		2	101	0.34	4.83×10^{-5}	0.067	127.48	0.028
		0	150	0.21	3.86×10^{-5}	0.079	242.82	0.032
	1	4	129	7.34	4.80×10^{-5}	0.020	0.594	0.014
		2	178	0.05	4.19×10^{-5}	0.025	106.09	0.010
		0	247	–	–	0.035	–	0.008
p-type	5	4 (5×10^{13} cm^{-2})	67	378	3.72×10^{-5}	0.079	0.136	0.012
		4	64	274	4.68×10^{-5}	0.055	0.130	0.023
		2	73	262	5.03×10^{-5}	0.085	0.212	0.036
		0	97	3.12	5.12×10^{-5}	0.092	19.107	0.039
	3	4	81	189	4.68×10^{-5}	0.042	0.142	0.017
		2	135	1.632	4.70×10^{-5}	0.052	20.315	0.021
		0	140	–	–	–	–	0.029
	1	4	219	0.38	4.66×10^{-5}	0.019	32.466	0.008
		2	243	–	–	0.100	–	0.012
		0	431	–	–	0.011	–	0.014
ITRS LP	5.1			295	5×10^{-5}	0.69	1.493	0.28

Because the optimal on-state current, I_{on}, cannot reach that of the ITRS demands at a gate length of $L_g = 5$ nm and UL = 4 nm, we test a high doping concentration of 5.0×10^{13} cm^{-2}, and the resulting transfer characteristics are plotted in Figs. 3 and 4.

In a logic switch, a high on-state current, one of the key figures of merit of the device's performance, implies a high operating speed. The on-state current, I_{on}, at different lengths of UL as a function of the gate length, L_g, is plotted in Fig. 5. As for the HP ML silicane devices, the on-state current increases as the gate length increases when UL = 4 nm, while the smallest on-state current is at $L_g = 3$ nm when UL = 0 and 2 nm. As for the LP devices, the on-state current increases as the gate length increases for all ULs. Given the same gate length, the on-state currents increase as the length of UL increases because of the increase of the effective channel length, and thus, the source-to-drain leakage is suppressed.

The on-state current of the *n*-type ML silicane HP MOSFET at $L_g = 5$ nm and UL = 4 nm (1374 μA/μm), with a doping concentration of 5.0×10^{13} cm^{-2}, can meet the ITRS goal of HP devices (900 μA/μm), while that of the corresponding *p*-type MOSFET (871 μA/μm) can meet 96.8% of the ITRS goal for HP devices. The on-state currents of the *n*-type ML silicane HP device are 5 times larger than that of the corresponding ML MoS_2 counterpart (230 μA/μm), while the on-state current of the *p*-type device is 1.5 times that of the corresponding ML MoS_2 counterpart (598 μA/μm) [40].

As for the LP devices, the on-state currents of the *n*-type silicane MOSFET at $L_g = 5$ and 3 nm (UL = 4 nm) are 438 and 467 μA/μm, respectively, and that of the *p*-type ML silicane MOSFET at $L_g = 5$ nm with a doping concentration of 5.0×10^{13} cm^{-2} is 378 μA/μm at UL = 4 nm; all of these values meet the ITRS goal for LP devices (295 μA/μm). Phonon scattering is not considered in our ballistic transport calculation. The electron temperature is set to 300 K, but the channel temperature is set to 0 K. According to previous reports [46–48], the on-state current including phonon scattering is degraded by 10%–25% compared with the ballistic transport limit when the channel length is less than 11 nm for 2D semiconductor MOSFETs. Thus, it is estimated that the on-state currents of the ML silicane devices with the inclusion of phonon scattering can also fulfill the ITRS requirement for both HP and LP devices.

The underlap region can make the channel barrier longer, thereby decreasing the transmission possibility and suppressing the short-channel effect. However, the gate-controlling capability of the uncovered channel region is weaker than that of the covered one, and too long an UL will degrade the performance of the device. These two conflicting aspects determine that the underlap should be optimized to achieve a high performance of the device. To clarify the effect of the UL more clearly, we calculate

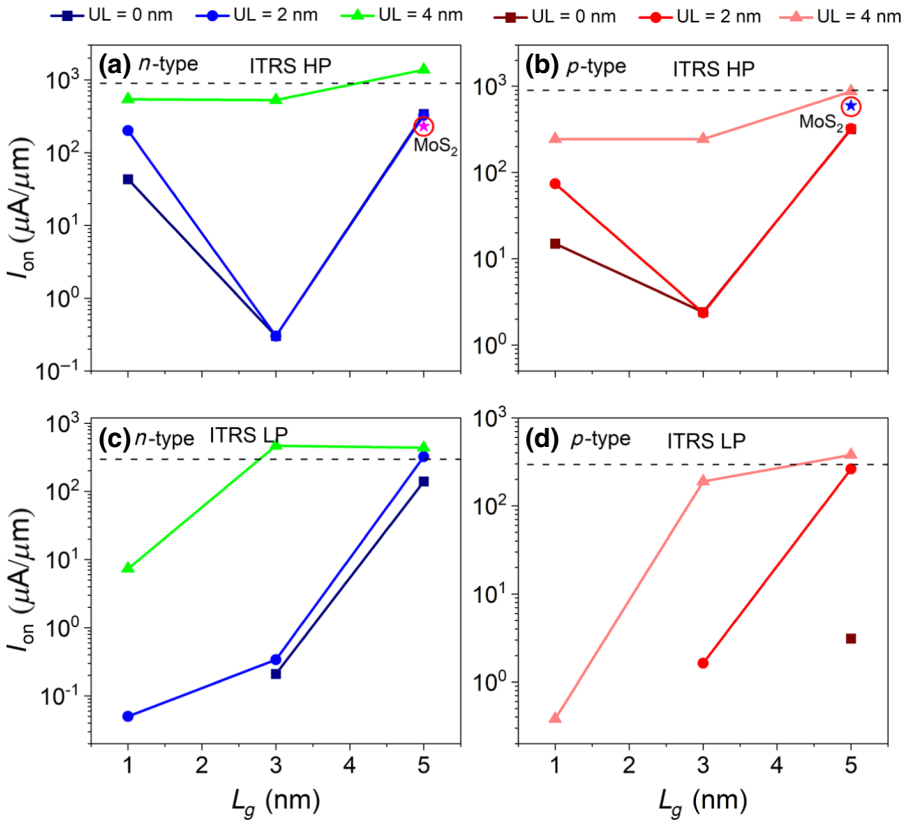

FIG. 5. (a)–(d) Benchmark of optimal I_{on} with different lengths of ULs versus L_g for n- and p-type sub-5-nm ML silicane HP and LP MOSFETs. Black dashed lines indicate ITRS HP and LP requirements for the on-state current. Stars denote the on-state current of ML MoS_2 FETs at $L_g = 5$ nm, which are taken from Ref. [30].

the local device DOS (LDDOS) of the ML silicane n-type HP MOSFET at $L_g = 5$ nm with different ULs, as shown in Fig. 6. We define the electron barrier height, Φ, as the energy barrier for the electron transferring from the CBM of the drain ($E = -0.35$ eV) to the source. The introduction of the UL makes the channel barrier longer, and therefore, the transmission possibility is smaller, which hinders tunneling leakage and probably favors the device performance. At the off state, with the same off-state current of 0.1 μA/μm, Φ is reduced from 0.61 eV at UL = 0 nm to 0.45 and 0.42 eV at UL = 2 and 4 nm, respectively. By applying a gate voltage of 0.66 V, the CBMs of the ML silicane in the channel region move downward, and the MOSFETs are changed into the on state. At the on state, Φ is zero at UL = 0 and 2 nm and it decrease to -0.18 eV at UL = 4 nm. Because of weak control of the gate to the UL part, compared with that to the overlap part in the channel, utilization of an UL larger than 4 nm is not always advantageous to the performance of the ML silicane devices.

The spectrum currents of the ML silicane MOSFETs in the on and off states with different ULs are shown in Fig. 6. The drain current, I_{DS}, is made up of the thermionic current, I_{therm}, and the tunneling current, I_{tunnel}, and it is divided into I_{therm} and I_{tunnel} by the CBM at the channel. The composition of the drain current, I_{DS}, is associated with the UL structure. The spectrum current is dominated by the tunneling current, I_{tunnel}, at UL = 0 nm, while a small part of the spectrum current comes from the thermionic current, I_{therm}, at UL = 2 nm and about half of the spectrum current comes from the thermionic current, I_{therm}, at UL = 4 nm due to the CBM gradually decreasing in the channel region at the off state. At the on state, the thermionic current, I_{therm}, predominates the spectrum current. The on-state peak of the spectrum current at UL = 4 nm (1.99×10^{-6} mA/eV) is larger those at UL = 0 (6.47×10^{-7} mA/eV) and 2 nm (1.22×10^{-6} mA/eV), leading to the increased on-state current. Such an increase is attributed to the fact that the density of states at the conduction band near the CBM in the drain region is increased at UL = 4 nm, since the drop of the CBM in the channel below μ_D ($\Phi = -0.18$ eV) leads to a compression of the states at the drain.

C. Gate control

The character indicating the ability of gate control of the FET in the subthreshold region is the SS, which impacts on the device performance and decides the operating voltage of the device. SS is defined as the increased gate voltage (V_g) used to change of the current by 1 dec of magnitude:

$$\text{SS} = \frac{\partial V_g}{\partial (l_g I_{DS})}. \tag{3}$$

A small SS indicates a better gate control ability. The lower limit of the SS for a MOSFET is 60 mV/dec at room

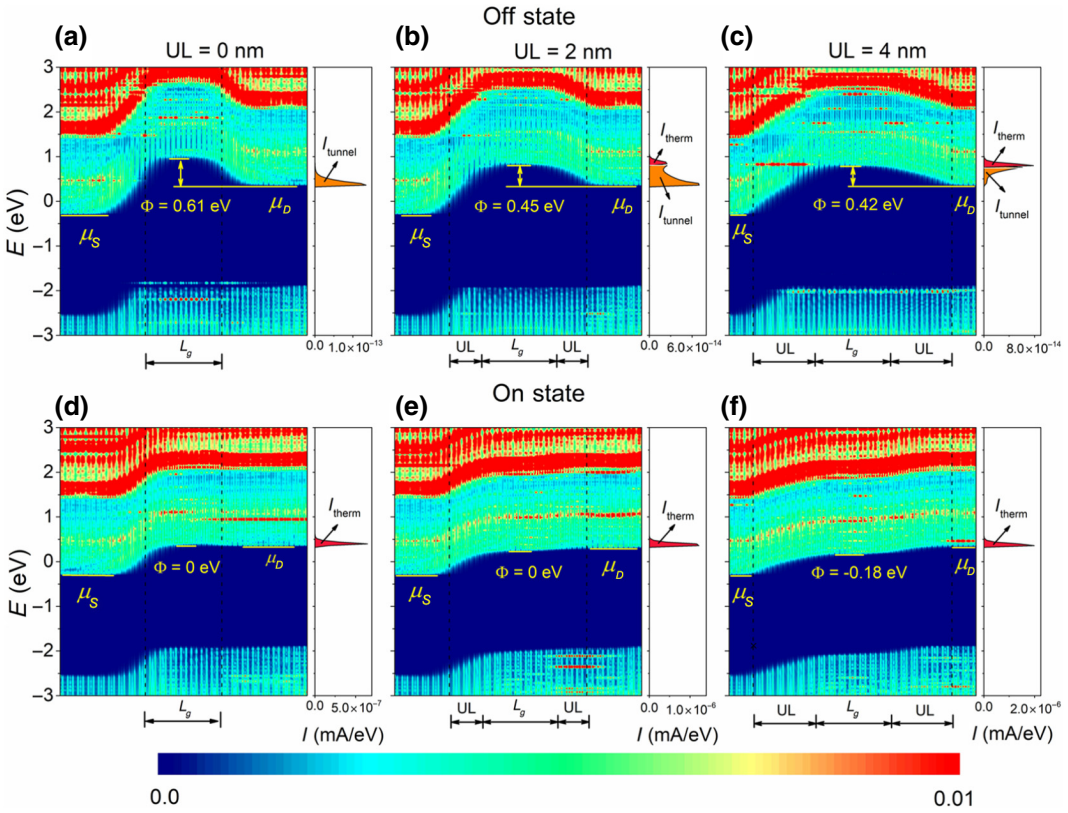

FIG. 6. Spatially resolved LDDOS and spectrum current of the *n*-type 5 nm DG ML silicane HP MOSFET with different lengths of UL at the off states (a)–(c) and on states (d)–(f). μ_S and μ_D are the electrochemical potentials of the source and drain, respectively. Φ is the energy barrier for electrons of the distribution tail at the CBM transporting from the drain to source. Units are 1/eV.

temperature. The calculated SSs at different gate lengths as a function of UL are plotted in Figs. 7(a) and 7(b). SS at $L_g = 1$ nm is about 1.5–3 times larger than that at $L_g = 3$ nm and about 2–4.5 times larger than that at $L_g = 5$ nm. It is apparent that SS decreases with an increase of the gate length, given the same UL. This increase is because the proportion of the gate length to the channel length increases with a longer gate length at the same UL, which improves the control ability of the gate.

With the same gate length, the subthreshold electrostatics is influenced by using the UL structures. It is found that SS decreases with an increase of UL. The UL = 2 nm results in a 20.7%–48.7% reduction of SS relative to the case with UL = 0 nm, except for the *p*-type ML silicane MOSFET at $L_g = 3$ nm with a reduction in SS of 3.6%. The UL = 4 nm results in a larger reduction of SS (28.1%–70%). The optimal SS is 64–65 mV/dec for the DG ML silicane MOSFET, which is close to the lower limit of thermionic devices at room temperature of 60 mV/dec, indicating a weak short-channel effect.

D. Effective delay time and power consumption

Switch time is a critical parameter for a digital circuit, which is generally measured by the effective delay time calculated as follows:

$$\tau = \frac{C_t V_{DD}}{I_{\text{on}}}, \tag{4}$$

where C_t is the total gate capacitance, V_{DD} is the supply voltage, and I_{on} is the on-state current. The total gate

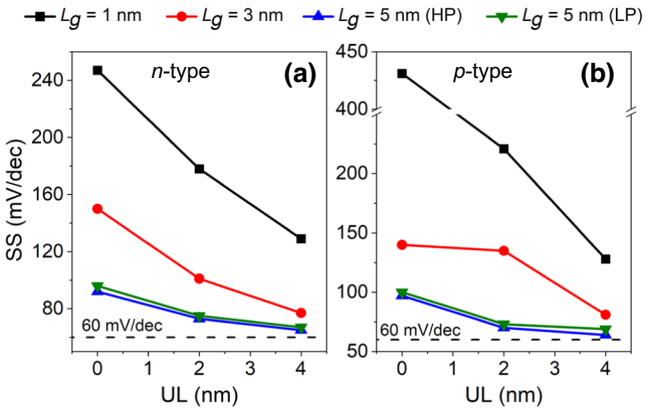

FIG. 7. SS as a function of UL length for (a) *n*-type and (b) *p*-type DG ML silicane MOSFETs with different gate lengths. Black dashed lines indicate the Boltzmann limit of 60 mV/dec for SS at room temperature.

capacitance includes the intrinsic gate capacitance, C_g, and the fringing capacitance, C_f. The fringing capacitance originates from the fringing fields emitted from the two sides (facing the source and drain) of the gate metal. According to the ITRS requirements, C_f is considered to be twice as much as C_g. C_g is defined as $C_g = \partial Q_{\rm ch}/\partial V_g$, where $Q_{\rm ch}$ is the calculated total charge for the central region. The total gate capacitances of the HP and LP devices are 0.019–0.210 and 0.011–0.133 fF/μm, respectively, which are lower than those of the corresponding HP (0.60 fF/μm) and LP (0.69 fF/μm) ITRS demands.

Figures 8(a) and 8(b) show the effective delay time that can fulfill the ITRS demands; detailed values for all devices are listed in Tables I and II. For the HP devices, the effective delay time of both the *n*- and *p*-type devices at $L_g = 1$ and 3 nm (0.527–169.08 ps) cannot reach the ITRS goal of 0.423 ps without an UL due to the small on-state current, while it is decreased to 0.024–0.110 ps, fulfilling the ITRS goal, with the UL of 4 nm. The effective delay time of all $L_g = 5$ nm HP devices (0.042–0.407 ps) meets the ITRS HP requirement. For the LP devices, only the effective delay time of the *n*-type device at $L_g = 5$ nm (0.620 ps) can meet the ITRS goal of 1.493 ps without an UL. By applying UL = 4 nm, the effective delay time of all devices (except for the *p*-type device at $L_g = 1$ nm) decreases to 0.054–0.594 ps, meeting the ITRS LP demands. The exception results from a low on-state current of 0.38 μA/μm.

Power consumption is a critical figure of merit to describe the switching energy of the devices. It is determined by the power-delay product (PDP), which is defined as PDP $= V_{DD} I_{\rm on} \tau = C_l V_{DD}^2$. As shown in Figs. 8(c) and 8(d), the PDP monotonously decreases with an increase of UL. For the HP devices, the PDPs of all devices examined at $L_g = 3$ and 5 nm (0.016–0.092 fJ/μm) can meet the ITRS HP goal of 0.28 fJ/μm, while the PDP at $L_g = 1$ nm (0.527–1.464 fJ/μm) is unable to meet the ITRS goal without an UL and it decreases to 0.024–0.051 fJ/μm with UL = 4 nm, fulfilling the ITRS goal. Remarkably, the PDPs of all examined LP devices (0.008–0.056 fJ/μm) are significantly lower than that of the ITRS LP goal of 0.24 fJ/μm, meeting the ITRS demands.

E. Discussion

A comparison of the performance metric limit of the sub-5-nm ML silicane FETs with the performance figures of metric of the experimental sub-10-nm Si Fin

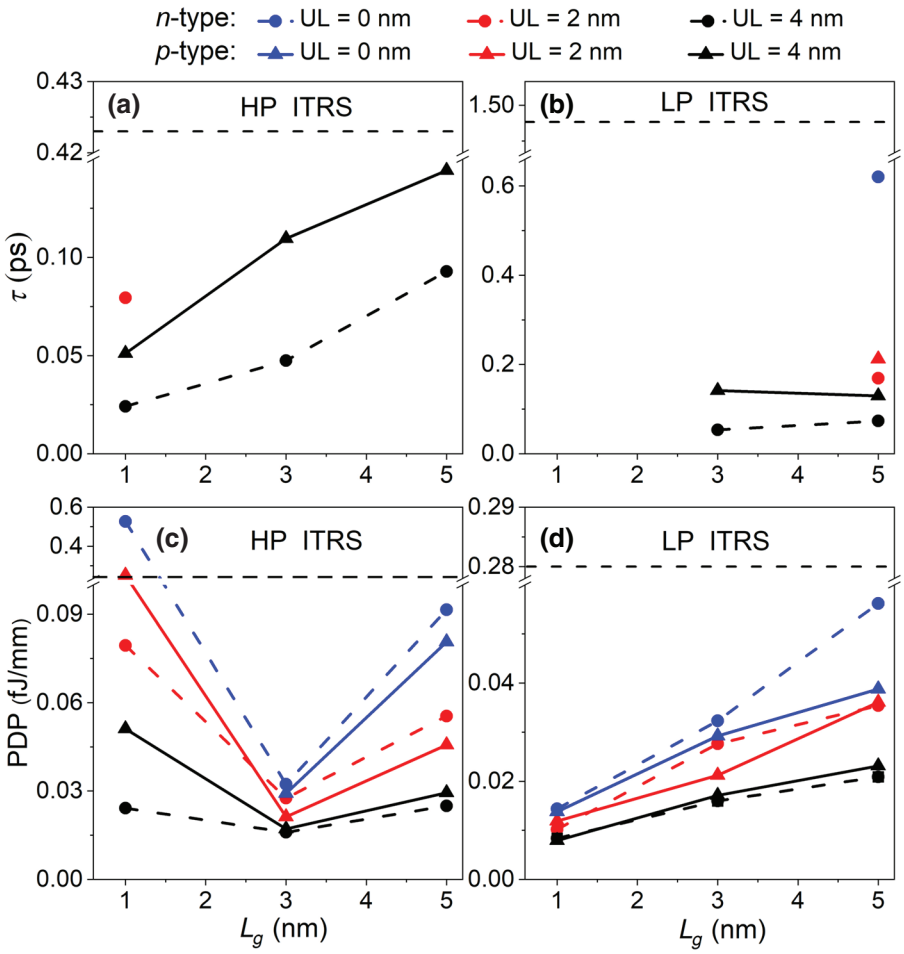

FIG. 8. Benchmark of (a),(b) the effective delay time and (c),(d) the power-delay product as a function of gate length in the sub-5-nm DG ML silicane MOSFET against the corresponding ITRS 2013 HP and LP requirements. Black dashed lines are the ITRS HP and LP requirements for the PDP and effective delay time. Only PDP and effective delay time of the DG ML silicane MOSFET that fulfill, or are close to, the ITRS requirements are shown.

TABLE III. Comparison of the upper performance metric limit of the sub-5-nm ML silicane HP DGFETs with $L_g = 5$ nm and UL = 0 nm in this work with the experimental limits of sub-10-nm Si Fin and UT SOI FETs. t_{ch} is the thickness of the channel materials. The on-state current, I_{on}, is taken from the I-V curve at $V_{DD} = 0.5$ V reported in the literature.

	L_{ch} (nm)	t_{ch} (nm)	V_{DS} (V)	V_g (V)	I_{on} (μA/μm)	I_{on}/I_{off}	Min SS (mV/dec)	Method
Si Fin [50]	10	17–26	0.5	0.5	≈50	5×10^2	125 ($V_{DS} = 1.2$ V)	Experiment
Si Fin [49]	5	14	0.5	0.5	≈100[a]	1×10^2	208 ($V_{DS} = 1.0$ V)	
UT SOI [51]	8	8 ± 2	0.5	0.5	≈100	1×10^3	83 ($V_{DS} = 1.2$ V)	
ML Silicane	5	0.37	0.5	0.5	258[b]	1.2×10^4	92 ($V_{DS} = 0.66$ V)	DFT + NEGF

[a]Because the minimum current is larger than 0.1 μA/μm, a gate range of (V_{th} − 0.2 V) to (V_{th} + 0.3 V) is applied instead of the ITRS standard.
[b]The on-state current at $V_{DS} = 0.5$ V is linearly derived from that at $V_{DS} = 0.66$ V.

and ultrathin Si-on-insulator (UT SOI) FETs is made in Table III. The performance upper limit of the ML silicane FETs is better than those of the experimental Si Fin and UT SOI FETs. The on-state current of the ML silicane FETs in the upper performance limit (258 μA/μm) is at least twice those for the Si Fin and UT SOI FETs (50–100 μA/μm) [49–51]. The minimum SS also decreases in the ML silicane devices, with an upper limit of 92 mV/dec, which is smaller than that of the Si Fin FET (125–208 mV/dec) and comparable to that of the UT SOI FET (83 mV/dec). The improved gate control of ML silicane is associated with its much smaller thickness (0.37 nm), compared with those in the Si Fin (14–26 nm) and UT SOI (8 ± 2 nm) FETs, and fewer traps at the ML silicane-dielectric interfaces. A characteristic length of the device, λ, considered as the distance of the electric field penetrating from the drain or source to the channel, is related to the thickness of the channel. According to the definition $\lambda = \sqrt{\alpha t_{ch} t_{ox} (\varepsilon_{ch}/\varepsilon_{ox})}$, in which t_{ch} (ε_{ch}) and t_{ox} (ε_{ox}) are the thickness (permittivity) of the channel material and the gate's insulating layer, respectively, and α is a constant related to the gate configuration with a value of 1/2 for the DG device structure [1,52]. The characteristic lengths of ML silicane, UT SOI, and Si Fin FETs are λ = 0.49, 1.99–2.57, and 3.0–4.15 nm, respectively. This difference also implies that the device performance of the Si Fin and UT SOI FETs can be further improved via further size scaling.

Silicane with various functional groups, such as benzyl-modified and phenyl-modified silicane, is fabricated in experiments [21,53]. Compared with those organo-modified silicanes, ML silicane, with hydrogen functional groups, has the thinnest thickness among silicanes. The reported thickness of ML silicane with an organic functional group is 1.11–1.62 nm in experiments [21,53]. Given the same permittivity of the channel materials as that of silicon, the characteristic lengths λ are 0.49 and 0.86–1.03 nm for the ML silicane with hydrogen and organic functional groups, respectively. Therefore, modulation of the gate for the organo-modified silicanes should be worse than that of the hydrogenated silicane.

The I_{on} values of the ML silicane MOSFETs at $L_g = 5$ nm are compared with those of recently reported appealing 2D semiconductors, such as ML black phosphorene (BP), MoS_2, arsenene, antimonene, and Bi_2O_2Se, from *ab initio* quantum transport simulations, as shown in Fig. 9. ML BP displays the largest I_{on} (4500 μA/μm) among these 2D semiconductors; however, poor stability hinders its large-scale application [40]. The ML silicane MOSFETs

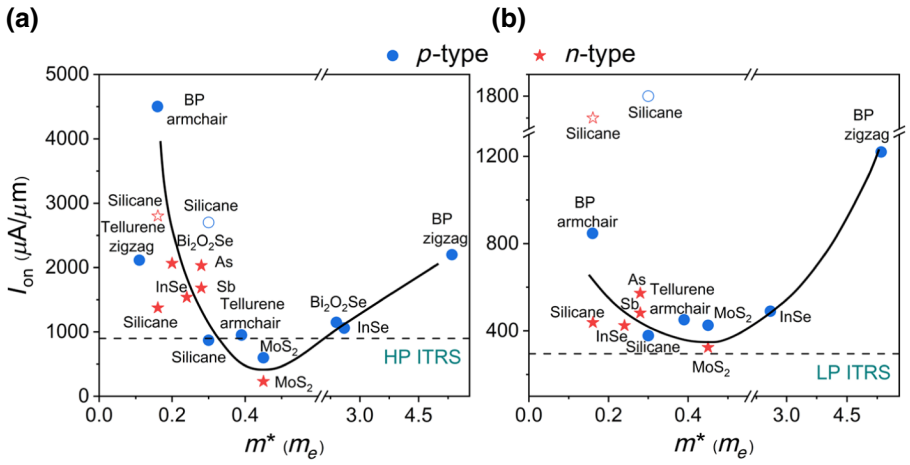

FIG. 9. On-state current of (a) HP and (b) LP devices versus effective mass, m^*, of ML 2D semiconductor channel materials along the transport direction at $L_g = 5$ nm for n- and p-type MOSFETs. Solid symbols represent data calculated from the quantum transport simulations [10,30,40,56–58], while open symbols represent data calculated from the SC method [27,28]. Black dashed lines indicate ITRS 2013 HP requirements. Solid black curves are guides to the eye.

have on-state currents, I_{on}, comparable with those of the ML arsenene, antimonene, Bi_2O_2Se, InSe, and tellurene MOSFETs. ML BP and InSe suffer from the same poor stability issue, and high-performance transistors of antimonene have not been fabricated in experiments [54,55]. Although I_{on} of ML Bi_2O_2Se HP MOSFETs at $L_g = 5$ nm is 2067 μA/μm, that of the counterpart LP MOSFETs is only 2.9 μA/μm, which is two orders of magnitude smaller than that of the ML silicane LP devices [30]. More importantly, ML silicane possesses an excellent advantage over other 2D semiconductor counterparts, which is superior compatibility with well-established silicon-based technology.

To interpret different I_{on} values of the 2D semiconductors transistors, the effect of the effective mass of the channel material on I_{on} is taken into consideration. A small effective mass along the transport direction has in two effects: (1) It gives rise to a large velocity of carriers along the transport direction, which is advantageous for obtaining a high on-state current [following the equation $I = Nev = NeI = Nev = Ne(eEt/m*)$, where N, v, E, and t are the number of carriers, the carrier velocity, the electric field, and relaxation time, respectively]. (2) It leads to a small DOS near the VBM or CBM [DOS $= (g_s g_v)/2\pi\hbar^2\sqrt{m_{\parallel}^* m_{\perp}^*}$, where g_s (g_v) is the spin (valley) degeneracies and $m_{\parallel}^*$ ($m_{\perp}^*$) is the effective mass along the transport (transverse) direction], which is not conducive to a high on-state current. The two effects compete with each other for the on-state current. Figure 9 plots the function of the on-state current versus the effective mass of different 2D semiconductors from previous studies [10,30,40,56–58]. It is found that the tendencies of I_{on} with the effective mass are similar in HP and LP devices at a gate length of 5 nm. I_{on} decreases as the effective mass increases when $0 < m^* < 0.45m_e$, in which carrier velocity plays a major role in the on-state current. I_{on} increases as the effective mass increases when $m^* > 0.45m_e$, in which the effect of DOS dominates for MOSFETS. Especially, ML BP possesses an anisotropic effective hole mass (0.16 and 5.4 m_e), which promises a large carrier velocity and adequate DOS synchronously [40]. Hence, a high on-state current is achieved. A large carrier velocity from a small effective mass benefits the I_{on} of both n- and p-type ML silicane MOSFETs.

The I_{on} values of HP and LP ML silicane MOSFETs calculated from the SC method are 2700–2800 and 1600–1700 μA/μm, respectively, at $L_g = 5.1$ nm, which are apparently higher than those (871–1034 and 378–438 μA/μm) obtained from the present *ab initio* quantum transport simulations by a factor of three to four [27,28]. Hence, the SE method overestimates I_{on} of both HP and LP ML silicane MOSFETs to a large extent. Such a discrepancy highlights the importance of *ab initio* quantum transport simulations in describing 2D FETs.

Applying a negative capacitance (NC) gate stack with ferroelectric materials can improve the device performance, which is reported in experiments [59–61]. Thus, we introduce a NC gate to the ML silicane MOSFETs to further improve the device performance, and the channel surface potential with the NC gate is amplified at a given V_g, which benefits a reduction of SS and the addition of I_{on}. The NC voltage (V_{NC}) originates from the Landau-Khalatnikov theory of ferroelectrics represented by [61,62]

$$V_{NC} = 2\alpha t_{FE} Q + 4\beta t_{FE} Q^3 + 6\gamma t_{FE} Q^5, \qquad (5)$$

in which α, β, and γ are the Landau coefficients of the ferroelectric layer with values of 1.911×10^8, 5.898×10^9, and 0 (SI units) for $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric materials, respectively. t_{FE} is the thickness of ferroelectric materials, and a 100-nm-thick ferroelectric layer is added to the ML silicane MOSFETs. Q is the electrical charge.

The corresponding SS and I_{on} of the ML silicane MOSFETs without and with NC dielectric are compared in Tables S1 and S2 within the Supplemental Material [45], respectively. Typically transfer characteristics of the n- and

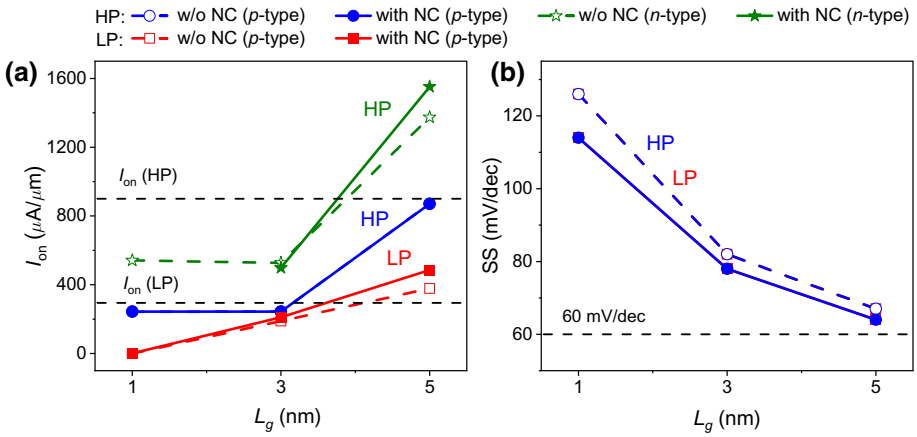

FIG. 10. Optimal on-state current (a) and SS (b) without (open symbols) and with (solid symbols) NC dielectric as a function of gate length for ML silicane MOSFETs.

p-type HP MOSFETs with and without NC at $L_g = 5$ nm and UL = 2 nm are plotted in Fig. S4 within the Supplemental Material [45]. The curve at the subthreshold region is apparently steep when applying the NC dielectric, and therefore, SS is reduced. We plot the optimal I_{on} and SS versus L_g of the sub-5-nm ML silicane MOSFETs without and with NC dielectric in Fig. 10. I_{on} is slightly affected by the NC dielectric, for example, the optimal I_{on} of the n-type ML silicane devices at $L_g = 5$ nm is increased from 1371 to 1551 μA/μm. The positive impact of the NC dielectric for SS is obvious, and the same effect is observed for HP and LP devices. SS of the p-type ML silicane MOSFET is improved from 126, 82, and 67 mV/dec to 114, 78, and 64 mV/dec at $L_g = 1$, 3, and 5 nm, respectively. The lowest SS of the ML silicane MOSFET is 62 mV/dec, which is close to the lower limit of 60 mV/dec at room temperature. Therefore, applying the NC technique to the ML silicane is a way to reduce SS and improve the device performance.

IV. CONCLUSION

Here, we explore the performance limit of DG sub-5-nm ML silicane MOSFETs by applying precise *ab initio* quantum transport simulations. The performances for both the HP and LP devices are improved with the use of an UL structure. The optimized on-state current of the n-type (p-type) ML silicane HP MOSFET is 1374 μA/μm (871 μA/μm) at $L_g = 5$ nm, meeting (nearly meeting) the ITRS requirements for a HP device, while that of the n-type (p-type) LP MOSFET is 438 μA/μm (378 μA/μm) at $L_g = 5$ nm and 467 μA/μm at $L_g = 3$ nm, achieving the ITRS demands for a LP device. The optimized n-type and p-type ML silicane FETs can also fulfill the ITRS requirements for an effective delay time and the PDP for both HP and LP devices for gate lengths down to 3 nm. Therefore, ML silicane is a promising channel material for the sub-5-nm transistor, owing to its high device performance and compatibility with current silicon-based technology. Very recently, a few-layer silicane FET has been realized by a solution process [63]. Owing to stacking defects and a large contact resistance, the silicane FET exhibits poor performance with an on:off ratio of about two and a hole mobility of 1.8 $cm^2\ V^{-1}\ s^{-1}$. An ideal silicane FET is urgently needed to be explored to improve the device performance, which requires much experimental effort.

ACKNOWLEDGMENTS

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